AMENDMENTS TO THE SPECIFICATION:

Please replac paragraph [0015] with the following amended paragraph:

[0015] That is to say, the present invention provides the step of forming first trenches in a semiconductor substrate, the step of forming isolation parts by filling in said first trenches with an insulating film, the step of forming trenches for forming wires so as to overlap, in a plane manner, said isolation parts and active regions which are surrounded by said isolation ~~part~~ parts, the step of forming an isolation film inside the trenches for forming said wires and the step of forming wires inside of said trenches for forming wires via said isolation film inside trenches, wherein in said step of forming trenches for forming wires, the corners of the bottom are rounded, and in said step of forming an isolation film inside the trenches part of, or all of, the insulating film is formed inside of the trenches through a deposition method.

Please replace paragraph [0028] with the following amended paragraph:

[0028] In addition, in accordance with the present invention, the depth of said first trenches finally becomes deeper than that of said secqnd second and third trenches.

Please replace paragraph [0047] with the following amended paragraph:

[0047] In addition, the semiconductor integrated circuit device of the present invention has trenches created in a semiconductor substrate, first semiconductor regions which are formed to extend up to a position deeper than said trenches in said semiconductor substrate, a gate insulating film formed inside said

trenches, gate electrodes formed inside said trenches via the gate insulating film, and semiconductor regions for the sources and drains formed on both sides of said gate electrodes, in a plane manner, in the semiconductor substrate, wherein said semiconductor regions for the sources and drains are formed to extend up to a position shallower than said first semiconductor regions, and second semiconductor regions, of which the ~~conductive~~ conductivity type is opposite to that of said first semiconductor regions, and third semiconductor regions, of which the ~~conductive~~ conductivity type is same as that of said second semiconductor regions, are formed to extend up to a position shallower than said second semiconductor regions, and the impurity concentration of said third semiconductor regions is higher than the impurity concentration of said second semiconductor regions.

Please replace paragraph [0069] with the following amended paragraph:

[0069] Fig. 11 (a) is a section diagram schematically illustrating the case wherein a gate insulating film is formed of ~~lay-ered~~ layered films through a thermal oxidation method and a CVD method, and Fig. 11 (b) is an enlarged cross-sectional view of the region E of Fig. 11 (a);

Please replace paragraph [0107] with the following amended paragraph:

[0107] In the following, the embodiments of the present invention will be described in detail with reference to the drawings. Here, elements having the same function throughout all of the drawings are all referred to by the same numerals and repetitive descriptions of them are omitted. In addition, in the present embodiments, a p channel type MIS·FET (Metal Insulator Semiconductor Field Effect Transistor) is abbreviated as pMIS, while an n channel type MIS·FET is

abbreviated as nMIS. In addition, in the present specification, an MIS·FET of an ordinary gate ~~electrodes~~ electrode structure refers to an MIS·FET with a structure having gate electrodes formed by patterning a conductive film deposited on the semiconductor substrate. In addition, in the present specification, a high concentration region is a region where the concentration of impurities which become donors or acceptors is comparatively high in comparison with a low concentration region. In addition, corner parts inside the trenches or angles of the bottoms inside the trenches include, in addition to angled parts formed between side surfaces and the bottoms inside the trenches, parts of which the radius of curvature is the smallest in the inside of the trenches.

Please replace paragraph [0110] with the following amended paragraph:

[0110] At this stage, the semiconductor substrate 1 is a semiconductor thin slate (so-called semiconductor wafer) ~~rdade~~ made of a p-type silicon single crystal, or the like, in, for example, approximately a circular plane form. And, for example, trench types of isolation parts (trench isolations) 2 are formed in the isolation regions. Those isolation parts 2 are the parts which perform the functions of element separation, separation within an element, or the like, and active regions L are formed in the regions surrounded by those isolation parts 2. The plane form of the active regions L has rounded parts on both edges in the memory cell region, as shown in Fig. 2, and is formed in a band form pattern extending in the diagonal direction.

Pl as r place paragraph [0111] with th following amended paragraph:

[0111] The method of formation of such isolation parts 2 is, for example, as follows. First, isolation trenches (first trenches) 2a, having a ~~of the~~ depth of approximately, for example, 350nm, are formed in the semiconductor substrate 1 through a photolithographic technology, a dry etching technology, and the like. The isolation trenches 2a are formed so that the width gradually spreads out from the bottom to the upper part. Accordingly, the inside surfaces of the isolation trenches 2a are inclined so as to be formed to have a forward taper. The inclination angle $\theta 1$ formed from the ~~inmer~~ inner surfaces of the isolation trenches 2a and the main surface, using the main surface of the semiconductor substrate 1 as a reference, is smaller than 90 degrees.

Please replace paragraph [0117] with the following amended paragraph:

[0117] Then, an insulating film 4 made of silicon oxide, or the like, having a thickness of approximately 10nm, is formed on the surface of the semiconductor substrate 1 by oxidizing the surface of the semiconductor substrate 1 through a thermal oxidation method, or the like, and, after that, a p well (first semiconductor region) 3P and an n well 3N are formed in the semiconductor substrate 1. The p well 3P and the n well 3N are formed by introducing separate impurities, respectively, using a separate photoresist (hereinafter referred to merely as resist) film as a mask, respectively, and, after that, by carrying out heat treatment. The p well 3P, wherein MIS·FETs for selecting memory cells are formed, is formed by implanting, for ~~exarqple~~ example, boron (B) at 300keV, 130keV and 40keV, respectively, in the amount of $1 \times 10^{13}/cm^2$, $2 \times 10^{12}/cm^2$ and $1 \times 10^{12}/cm^2$ and, after that, by carrying out a heat treatment at, for example, 1000°C for 30

minutes. Here, for example, phosphorous (P) or arsenic (As) is introduced in the n well 3N.

Please replace paragraph [0119] with the following amended paragraph:

[0119] Next, as shown in Fig. 3, an insulating film 5 made of silicon nitride (Si_3N_4, or the like, hereinafter the same) of the thickness of, for example, approximately 50nm, is formed on the main surface of the semiconductor substrate 1 through a CVD (chemical vapor deposition) method, or the like. Then, a resist film 6a is formed on the insulating film 5. As for the plane form of the resist film 6a, a pattern ~~si~~ is formed wherein word line (wire) formation regions are exposed and other regions are covered. Here, a reflection preventive film may be applied between the insulating film 5 and the resist film 6a. After that, as shown in Fig. 4, the insulating films 5 and 4, as well as the insulating film 2b, are removed through etching in sequence by using the resist film 6a as a mask (in the case that the reflection preventive film exists, the reflection preventive film is also removed). Thereby, trenches (second trenches, trenches for forming wires) 7a are formed in the isolation parts 2 in the semiconductor substrate 1. The depth of these trenches 7a is shallower than the isolation trenches 2a of the isolation parts 2. The depth of trenches 7a is set so that the insulating film 2b remains at the bottom of the trenches 7a even after the insulating film 2b is slightly shaved, since it is shaved in a later described step.

Please replace paragraph [0129] with the following amended paragraph:

[0129] In addition, in the present Embodiment 1, the gate trenches are formed through the above-described step etching method, and, thereby, the

undercuts beneath the hard mask can be prevented and trenches of a desired depth which have a large radius of curvature of the bottom corners of the above-described trenches can be obtained. Thereby, the characteristics of the MIS·FETs of a buried gate electrode structure, especially the sub-threshold characteristics, can be increased (sub-threshold coefficient can be made smaller). That is to say, the divergence of the electric field in the vicinity of the bottom corners within the trenches 7b can be relaxed so that the channel resistance can be reduced and a desired drain current can be obtained at a predetermined threshold voltage. Therefore, it becomes possible to increase the element driving performance. In addition, it becomes unnecessary to make the transistors of the ~~depression~~ depletion type, and, therefore, the increase of the leakage current can be prevented, and it also becomes possible to prevent an increase of power consumption. In the present Embodiment 1, the radius of curvature of the bottom corners within the trenches 7b is made to be, for example, 10nm or more, or, for example, approximately 30nm. The radius of curvature in the bottom corners within the trenches 7b will be described in more detail later.

Please replace paragraph [0133] with the following amended paragraph:

[0133] After that, as shown in Fig. 15, after an insulating film 10 made of, for example, silicon nitride, is deposited through a CVD method, or the like, by etching back the insulating film 10 through an isotropic dry etching method, an insulating film 10 is filled in the voids on the upper surface of the gate electrode forming film 9a, which is filled into the trenches 7a and 7b, as shown in Fig. 16. At this time the insulating film 10 is supposed not to leave a residue on the upper side walls of the trenches 7a and 7b.

Please r plac paragraph [0134] with the following amended paragraph:

[0134] Next, as shown in Fig. 17, the gate electrode forming film 9a is, again, etched back through an isotropic dry etching treatment. At this time, the insulating film 5 on the semiconductor substrate 1 and the insulati ng film 10, which is filled in the voids of ~~date~~ gate electrode forming film 9a, are used as an etching mask. The reason why the insulating film 10 is formed in the voids in this way is that, if the insulating film 10 does not exist, the etching proceeds more in the void parts than in other parts at the time of the etching back treatment of the gate electrode forming film 9a, and, therefore, the gate insulating film 8b is exposed so as to include the risk of defects. Accordingly, in case such a problem doesn't occur, the step of formation of the insulating film 10 may be eliminated. Then, an oxidization process is applied to the semiconductor substrate 1 and, thereby, amorphous silicon is oxidized, and, after that, the part oxidized by this is removed by hydrofluoric acid, or the like. Thereby, it becomes possible to remove the residue of amorphous silicon even if it remains within the trenches 7a and 7b. After that, as shown in Fig. 18, a conductive film 11 made of, for example, titanium (Ti), or the like, is deposited through a CVD method, a ~~spattering~~ sputtering method, or the like, and then the conductive film 11 and the gate electrode forming film 9a cause a silicidation reaction through the process of annealing. After that, by removing the conductive film 11, which hasn't reacted, using hydrogen peroxide, or the like, word lines WL (gate electrodes 9) made of, for example, titanium silicide, or the like, are formed within the trenches 7a and 7b, as shown in Figs. 19 and 20. In the present Embodiment 1, microscopic trenches 7a and 7b are filled in with amorphous silicon which makes an effective filling in possible, and, after that, the amorphous silicon is made to be silicide through silicidation, and, thereby, the gate electrodes 9 made of

titanium silicide, or the like, which is of low resistance, can be formed within the trenches 7a and 7b in an effective filled in manner. Here, the filled in gate electrode material is not limited to titanium silicide, but, rather, can be changed in a variety of ways. For example, the surface of the titanium silicide can be further nitrided so as to gain a structure where titanium nitride is layered. In this case, it becomes possible to increase the withstanding characteristics of the gate electrode at the time of the cleaning treatment after contact holes are created in the insulating film so that gate electrodes are exposed in the later steps. In addition, by using metal, such as tungsten, the resistance of the word lines WL can be reduced to a great extent. Furthermore, a structure can be gained wherein, for example, a polycrystal silicon of low resistance, tungsten nitride and tungsten are stacked in this order from the lower layer. In this case, by making the lowest layer of polycrystal silicon p-type, the threshold voltage can be made larger by the difference of work function with the n-type silicon, and, therefore, it becomes possible to secure a desired threshold voltage under the condition where the impurity concentration of the semiconductor substrate 1 is made lower. This effect can be gained in the case where tungsten is used as a gate electrode material. In addition, the gate ~~electrodes.may~~ electrodes may be constructed of, only, a polycrystal silicon of low resistance.

Please replace paragraph [0135] with the following amended paragraph:

[0135] In addition, in the present Embodiment 1, it is preferable that the top surfaces of the word lines WL (gate electrodes 9) are formed in locations 40nm, or more, deeper than the main surface of the semiconductor substrate 1. Though it is not particularly limitative in the present Embodiment 1, the top surfaces of the word lines WL are formed at positions, for example, approximately 70nm

deeper than the main surface of the semiconductor substrate 1. The reason for this will be described later. In addition, Fig. 20 shows a plan view of the main part of the memory cell region. The word lines WL are arranged so as to cross the ~~a ctive~~ active regions L. Two word lines WL are arranged so as to overlap in a plane over one active region L. The part in a word line WL which overlaps in a plane over an active region L becomes a gate electrode 9. Here, the active regions L are arranged diagonally relative to the extending direction of the word lines WL.

Please replace paragraph [0136] with the following amended paragraph:

[0136] Next, after an insulating film 12 made of, for ~~example; silicon~~ example, silicon oxide is deposited on the semiconductor substrate 1 through a CVD method, or the like, the insulating film 12 is polished through a CMP method, or the like, using the insulating film 5 as an etching stopper. Then, the remaining insulating film 5 is removed using heated phosphate and, thereby, a cap insulating film 12a made of, for example, silicon oxide is formed on the word lines WL (gate electrodes 9) as shown in Fig. 21. At this stage, as shown in Fig. 22, the insulating film 2b of the isolation parts 2 remains in the lower part of the word lines WL (gate electrodes 9) within the trenches 7a. This is for the purpose of controlling or preventing parasitic elements from being formed, since parasitic elements are formed using the word lines WL as its parts when the thickness of the insulating film 2b secured on the bottom side of the trenches 7a is too thin. As a result of the investigation by the present inventors, it is ~~prefe rable~~ preferable that the thickness d of the insulating film 2b is, for example, approximately 100nm or more. In addition, the depth of the trenches 2b of the isolation parts 2 is formed to be deeper than the trenches 7a and 7b in order to secure the desired element isolation performance.

Please replac paragraph [0141] with the following amended paragraph:

[0141] Next, after depositing an insulating film 20 made of silicon oxide having a thickness of, for example, approximately 100nm on the main surface of the semiconductor substrate 1, the top surface is made flat by polishing the above through a CMP method. Then, as shown in Figs. 25 and 26, contact holes 21 are formed in the insulating film 20 so as to expose the semiconductor regions (low concentration regions 15a) for the sources and drains of the MIS·FET (MIS·FET for memory cell selection of a buried gate electrode ~~structures Fig. 26~~ structures. Fig. 26 shows a plan view of the main part of the memory cell region in the step of Fig. 25. The contact holes 21 are formed, for example, in a plane circular form and are arranged at positions overlapping the active regions L in a plane between word lines WL (gate electrodes 9) neighboring each other. That is to say, the contact holes 21 are arranged so as to overlap on both ends and in the center of ~~the, active~~ the active regions L in a plane manner. After that, a polycrystal silicon to which, for example, phosphorous is doped, is deposited on the semiconductor substrate 1 and, after that, an annealing treatment is carried out for activating the impurities. At this time, impurities, (phosphorous) are diffused into the semiconductor substrate 1 from the plug 22, and, thereby, high concentration regions are formed in the semiconductor regions for sources and drains of a MIS·FET having a buried gate structure. After that, the polycrystal silicon film is polished through a CMP method, or the like, so as to leave only the portion within the contact holes 21, and, thereby, plugs 22 are formed within the contact holes 21. Fig. 27 shows an enlarged view of a MIS·FET (MIS·FETQs for memory cell selection) part of a buried gate electrode structure in the semiconductor substrate 1 after the above step. The source and drain regions of MIS·FETQs for memory cell selection have low concentration

regions 15a and high concentration regions 15b formed in the upper part thereof. The borders between the low concentration regions 15a and the p well 3P are formed at positions deeper than the top surface of the gate electrodes 9 (word lines WL) of a buried type. In addition, the borders between the high concentration regions 15b and the low concentration regions 15a are formed at positions shallower than the top surface of the gate electrodes 9 (word lines WL) of a buried type. These high concentration regions 15b are formed through the diffusion of impurities from the plugs 22. Capacitor elements for information storage are electrically connected to one type of plug 22 (that is to say, high concentration regions 15b) while bit lines are electrically connected to the other type of plug 22 (that is to say, high concentration regions 15b).

Please replace paragraph [0142] with the following amended paragraph:

[0142] Next, as shown in Fig. 28, an insulating film 23 made of, for example, silicon oxide is deposited on the semiconductor substrate 1 through a CVD method, or the like, of which the top surface is then made flat through a CMP method, or the like, and, after that, through holes 24a, which expose the top surfaces of the plugs 22, are formed in the insulating film 23, and contact holes 24b which expose the semiconductor regions 17 and 18 for the sources and drains of nMISQn and pMISQp in the ~~phosphorous~~ peripheral circuit region ~~a re~~ are formed in the insulating films 23 and 20. Then, for example, titanium and titanium nitride are deposited on the semiconductor substrate 1 in this order from the lower layer through a ~~spattering~~ sputtering method, a CVD method, or the like, and, after that, tungsten, or the like, is deposited through a CVD method, or the like. Titanium and titanium nitride have functions as a barrier film for preventing tungsten and silicon

from reacting during the heat treatment in the following capacitor formation steps. After that, the plug 25 is formed in through holes 24a and contact holes 24b by polishing a layered film, such as titanium, titanium nitride and tungsten, through a CMP method, or the like. At this time, the insulating film 23 functions as a stopper. After that, an insulating film 27a made of, for example, silicon oxide is formed on the insulating film 23, and, after that, trenches for forming wires are formed in the former film. Then, on top of this, a conductive film, such as tungsten, is deposited through a ~~spattering~~ sputtering method, or the like, and, after that, by polishing the above through a CMP method, or the like, bit lines BL and the first layer wires 26 of a buried type are formed. Here, a plan view of the main part of the memory cell region at this stage is shown in Fig. 29. The bit lines BL extend in the direction perpendicular to the word lines WL in a plane manner and are arranged so as to overlap the contact holes 21 in the middle of the active regions L in a plane manner.

Please replace paragraph [0143] with the following amended paragraph:

[0143] Next, As shown in Fig. 28, after depositing an insulating film 27b made of, for example, silicon oxide on the semiconductor substrate 1 through a CVD method, or the like, an insulating film 28 made of, for example, silicon nitride is further deposited thereon. Then, through holes 29 for connecting the lower electrodes of the capacitors and plug 22 are formed in the insulating film 28, and, after that, an insulating film 30 made of, for example, silicon oxide is deposited on the insulating film 28 through a CVD method, or the like. After that, capacitor holes 31 are created in the insulating film 30. At this time, by carrying out etching under the condition that silicon oxide has a higher etching rate than silicon nitride, the insulating films 23 and 27, which are ~~expose d~~ exposed from the through holes 29

at the bottoms of the capacitor holes 31, are removed through etching using the insulating film 28 as a mask, and, thereby, through holes 32 which expose the top surfaces of the plugs 22 are formed.